

**Amendments to the Claims**

This listing of claims will replace all prior versions and listings of claims in the application.

1. (Currently amended) An electronic component comprising:

an electronic device package formed from an integral silicon wafer having a recess, the recess including a single conductive region, the wafer and the conductive region conductively coupled so as to be at substantially the same electrical potential;

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess and physically coupled to the package by a conductive bonding material, and wherein the non-top terminal is electrically coupled to the conductive region by the conductive bonding material; and

a dielectric material disposed so as to form a planar surface over the recess that is level with or higher than the top of the device, the dielectric material filling the recess not occupied by the device and conductive bonding material.

2. (Previously Presented) An electronic component according to claim 1, wherein:

the conductive region is formed by metallization.

3. (Cancelled)

4. (Original) An electronic component according to claim 1, wherein the conductive region comprises:

- a first layer of titanium;
- a second layer of copper deposited on the first layer; and
- a third layer of chrome deposited on the second layer.

5. (Cancelled)

6. (Cancelled)

7. (Previously Presented) An electronic component according to claim 1, further comprising:

- a plurality of metallized bumps in a plane, wherein each terminal is electrically coupled to at least one bump, and each bump is electrically coupled to at most one electrically distinct terminal.

8. (Original) An electronic component according to claim 7, wherein:

- the package includes a top and a bottom; and
- the bumps are located above the top of the package.

9. (Previously Presented) An electronic component according to claim 1, wherein the device is a vertical device and the bottom of the device is coupled to the recess.

10. (Original) An electronic component according to claim 1, further comprising:  
a second conductive region coupled to a terminal other than the non-top terminal.

11. (Original) An electronic component according to claim 1, a plurality of contacts including at least a first contact and a second contact, the first contact being electrically coupled to the non-top terminal and the second contact being electrically coupled to a terminal other than the non-top terminal.

12. (Original) An electronic component according to claim 11, wherein the plurality of contacts reside in the same plane.

13. (Previously Presented) An electronic component according to claim 11, further comprising:

a second layer of dielectric completely covering the silicon wafer and the device except for the plurality of contacts.

14. (Currently amended) An electronic component comprising:

an electronic component package formed from an integral silicon wafer having a recess, the recess including a first and only conductive region, the wafer and the first conductive region conductively coupled so as to be at substantially the same electrical potential; and

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal and a top terminal, the device being disposed in

the recess and physically coupled to the package by a conductive bonding material, wherein the non-top terminal is electrically coupled to the first conductive region by the conductive bonding material, and the top terminal is electrically coupled to a second conductive region; and

a dielectric material disposed over the recess such that at least a portion of the first and second conductive regions are essentially planar, the dielectric material filling the recess not occupied by the device and conductive bonding material .

15. (Original) An electronic component according to claim 14, wherein:

the second conductive region is a solder bump.

16. (Currently amended) An electronic component comprising:

an electronic device package formed from an integral silicon wafer having a recess, the recess including a single conductive region, the wafer and the single conductive region conductively coupled so as to be at substantially the same electrical potential;

an electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal located in a region other than the top of the device, the device being disposed in the recess and physically coupled to the package by a conductive bonding material, wherein the non-top terminal is electrically coupled to the conductive region by the conductive bonding material; and

a layer of insulation disposed so as to form a planar surface over the recess that is level with or higher than the top of the device, the layer of insulation filling the recess not occupied by the device and conductive bonding material.

17. (Original) An electronic component according to claim 16, wherein:

one of the terminals of the device is a top contact located at the top of the device;  
and

the package has a package top, wherein the package top also includes a contact coupled electrically via the conductive region to the non-top terminal.

18. (Previously Presented) A component according to claim 16, wherein:

the conductive region comprises a layer of metal; and  
the electronic device resides within the recess and the metal is electrically coupled to the non-top terminal of the device.

19. (Cancelled)

20. (Original) An electronic component according to claim 18, wherein the metal of the conductive region extends to a portion of the package top, the electronic component further comprising:

a bottom contact electrically coupled to the metal on the package top.

21. (Currently amended) An electronic component comprising:

an electronic device having a first terminal and a second terminal, wherein a first dimension is defined therebetween;

an electronic device package having a first surface, the package formed from an integral silicon wafer having a recess on the first surface that has a depth that is substantially equal to the first dimension, the package further having a layer of metal applied to the recess and to a portion of the first surface, wherein the electronic device resides within the recess and is physically coupled to the package by a conductive bonding material, the second terminal is electrically coupled to the layer of metal by the conductive bonding material, and the layer of metal and the wafer are conductively coupled so as to be at substantially the same electrical potential; and

a layer of insulation disposed so as to form a planar surface over the recess that is level with or higher than the top of the device, the layer of insulation filling the recess not occupied by the device and conductive bonding material.

22. (Previously Presented) An electronic component according to claim 21, further comprising:

a first contact coupled to the first terminal; and

a second contact coupled to the metal residing on the first surface of the package.

23. (Withdrawn) A method of packaging an electronic device to create an electronic component, the electronic device having a top terminal and a bottom terminal, a first dimension being defined by the distance between the top terminal and the bottom terminal, the method comprising:

creating a recess in a silicon wafer, the recess having a depth substantially equal to the first dimension of the electronic device;

applying a conductive material to the recess;

inserting the electronic device into the recess so that the bottom terminal is coupled to the conductive material;

applying a dielectric into the recess;

applying a top contact electrically coupled to the top terminal of the electronic device; and

applying a bottom contact electrically coupled to the conductive material.

24. (Withdrawn) An electronic component according to claim 23, wherein the step of applying the conductive material comprises:

applying a first layer of titanium;

applying a second layer of copper on the first layer; and

applying a third layer of chrome on the second layer.

25. (Withdrawn) An electronic component according to claim 23, wherein the step of applying the dielectric into the recess comprises:

applying a dry etch bisbenzocyclobutene dielectric;

removing the dry etch bisbenzocyclobutene dielectric from the top terminal and a part of the conductive layer;

applying a photo defineable bisbenzocyclobutene dielectric; and

exposing the top terminal and the part of the conductive layer.

26. (Withdrawn) The method according to claim 23, wherein:

the silicon wafer has a top and a bottom, the recess being created on a portion of the top, and wherein the bottom contact is located on the top of the silicon wafer to enable surface mounting.

27. (Withdrawn) The method according to claim 26, wherein multiple recesses are created on a single silicon wafer and electronic devices are each inserted into one of the multiple recesses.

28. (Withdrawn) The method according to claim 27, wherein at least one of the electronic devices is a resistor, diode, capacitor, or inductor.

29. (Withdrawn) The method according to claim 27, the method further comprising:  
cutting the silicon wafer to form multiple electronic components.

30. (Withdrawn) The method according to claim 29, further comprising:  
prior to the step of cutting, testing each of the electronic components.

31. (Withdrawn) The method according to claim 23, wherein:  
the electronic component is a ball grid array packaged component.



32. (Previously presented) An electronic component comprising:

a non-molded electronic component package having a package top and formed from an integral silicon wafer including a recess;

a bare die electronic device having a top, a bottom, sides, and a plurality of contacts, the device being disposed in the recess and physically coupled to the package by a conductive bonding material, wherein at least one of the plurality of contacts is electrically coupled by the conductive bonding material to a metallization layer, the wafer and the metallization layer conductively coupled so as to be at substantially the same electrical potential; and

a planarizing material filling the recess not occupied by the device and conductive bonding material to substantially create a level plane that includes the package top.

33. (Cancelled)

34. (Cancelled)

35. (Previously presented) An electronic component according to claim 32, further comprising:

a second metallization layer coupling one contact to a redistribution point on the package top, wherein each contact remains electrically distinct.

36. (Original) An electronic component according to claim 35, further comprising:

a plurality of conductive bumps, each bump being disposed at a redistribution point.

37. (Withdrawn)

38. (Withdrawn)

39. (Withdrawn)

40. (Previously presented) An electronic component comprising:

an electronic device package formed from an integral silicon wafer having a recess, the recess including a single conductive region, the wafer and the conductive region conductively coupled so as to be at substantially the same electrical potential;

a bare die electronic device having a top, a bottom, sides, and a plurality of terminals, including a non-top terminal, the device being disposed in the recess and physically coupled to the package by a conductive bonding material, and wherein the non-top terminal is electrically coupled to the conductive region by the conductive bonding material;

a planarizing material filling the recess not occupied by the device and conductive bonding material to substantially create a level plane that includes the package top; and

a plurality of contacts including at least a first contact and a second contact, the first contact being electrically coupled to the non-top terminal and the second contact

being electrically coupled to a terminal other than the non-top terminal, wherein the plurality of contacts reside in the level plane.

41. (Previously presented) An electronic component according to claim 10 wherein the second conductive region is non-wire bonded.

42. (Previously Presented) An electronic component according to claims 16, wherein the layer of insulation is a dielectric.

43. (Previously Presented) The electronic component according to claim 36, such that the conductive bumps are spaced for electrically coupling with a pre-printed circuit board.

44. (Previously Presented) The electronic component according to claim 43, wherein the electronic component is a flip chip.

45. (Currently amended) An electronic component comprising:

a silicon wafer having a recess;

a bare die electronic device having first and second contacts, the device being disposed in the recess and physically coupled to the wafer by a conductive bonding material, the first contact electrically coupled by the conductive bonding material to an electrically conductive region, the electrically conductive region electrically coupling the first contact and the wafer to an electrical input of the electronic component, wherein the

second contact is electrically coupled by non-wire bonding to a second electrical input of the electronic component, and

a dielectric material disposed so as to form a planar surface over the recess that is level with or higher than the top of the device, the dielectric material filling the recess not occupied by the device and conductive bonding material.

46. (Cancelled)

47. (Previously Presented) An electronic component according to claim 45, wherein the bare die electronic device is covered by the dielectric material and the electronic component is a flip chip.

48. (Previously Presented) The electronic component according to claim 47, wherein the silicon wafer is an integral piece of silicon.